**Performance of Differential Lines based on SMIC55LL Process using 3D EM Simulations**

**Content**

1. **Introduction**
2. **Conventional Differential Lines designed for the Tape-out**
3. **Conventional Differential Lines with different silicon conductivity**
4. **Differential Lines with Floating Patterned Shield**
5. **Differential Lines with Floating Patterned Shield with Split Lines**
6. **Modeling**
7. **Introduction**

The purpose of this document is to present the performance of differential Lines based on SMIC Process55LL. We will show some other topologies of Lines dedicated to improve the performances of conventional differential Lines designed using the SMIC PDK.

In this study, I will focus on one set of parameters for the differential Line that has been designed in one of our Tape-out in Oct 2014. The parameters are described in Tab. 1. The 3-D representation of the differential Line is shown in Fig. 1. Note that all the results will be reported for a normalized length of line of 1mm.

Tab. 1. Default set of parameters for our 3-D ElectroMagnetic simulation.

|  |  |  |
| --- | --- | --- |
| Width | W | 14.54um |
| Spacing | S | 8.63um |
| Length | L | 500um(\*)(\*\*) |
| Metal of the Lines | Met | TM2 (5.5Ohms/sq) |
| Conductivity of the Lossy Silicon | Ro\_Si | 10S/m |
| Frequency Range | Freq | 0.1-10GHz |

(\*) Note that on the layout Tape-out in Oct 2014 L~1.8mm.

(\*\*)This length is normalized to 1mm in our study.

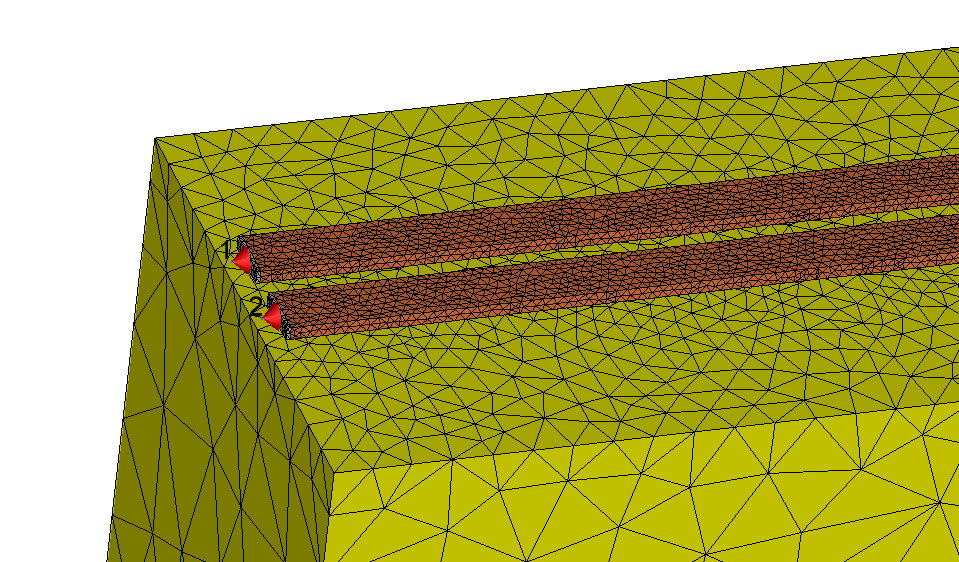


Fig. 1: 3-D Representation of the Conventional Differential Line

The simulation is set using 4 ports connected to each extremity of the metal Lines. All impedance ports in this document will refer to 50.

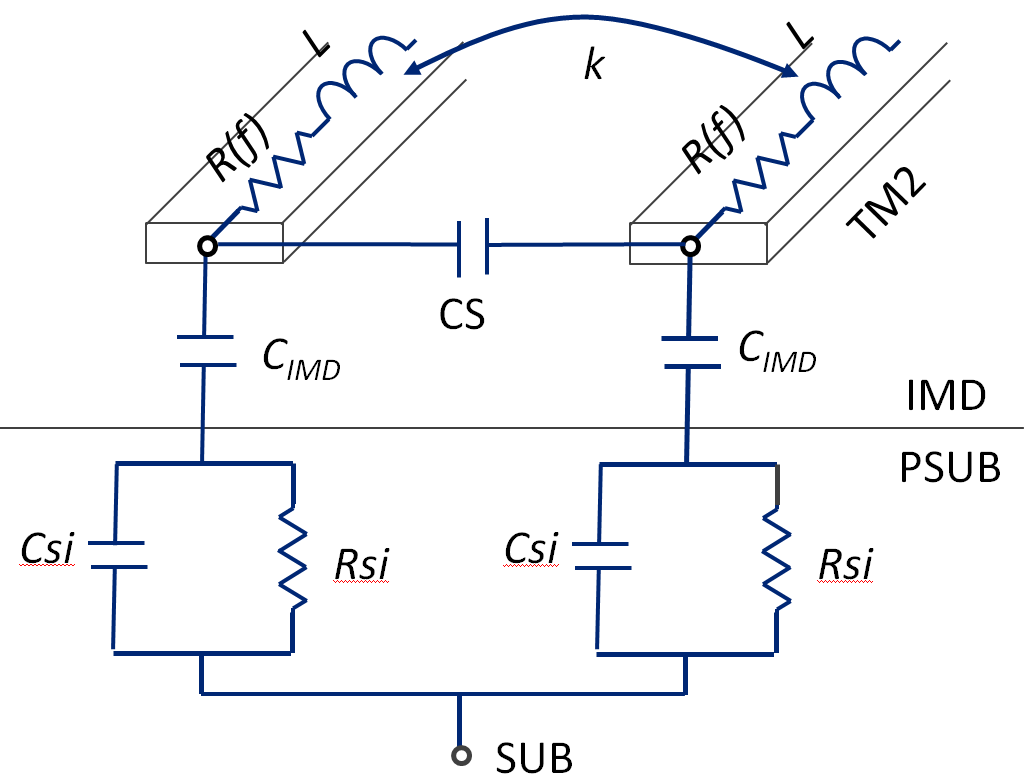


Fig. 2: Electrical Representation of the Conventional Differential Line

Note that this document will not discuss about the optimization of the width and the spacing to get the good matching of the line with the considered impedance of the circuit. This topic is out of scope.

Furthermore, the document will propose some ways to improve easily the performance of designed Line without providing the best optimal Line that will require more investigation. This point is highly dependent of the considered circuit and of its input/output impedance.

This study is based on Montage’s background experiences on the optimization of inductive devices.

1. **Conventional Differential Lines designed for the Tape-out**

We will consider in this first part, the Differential Line shown in Fig. 1, with the parameters described in Tab.1. The first result consists to extract the losses of the Line versus frequency in differential mode. The representation of the simulated schematic is shown in Fig. 3. The results are presented in Fig. 4.

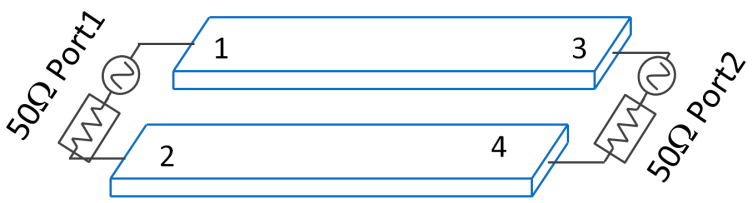


Fig. 3: First simulated representation of the Line in Differential mode in order   
to extract the losses of the line.

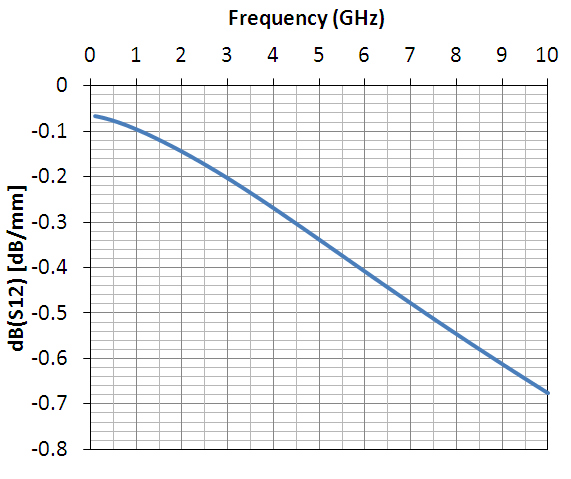


Fig. 4: Losses dB(S12) (dB/mm) versus Frequency (GHz).

The losses extracted are evaluated to 0.17dB/mm 0.33dB/mm at 2.45GHz and 4.9GHz, respectively. These performances consider that the silicon substrate features a conductivity of 10S/m or a resistivity of 10.cm.

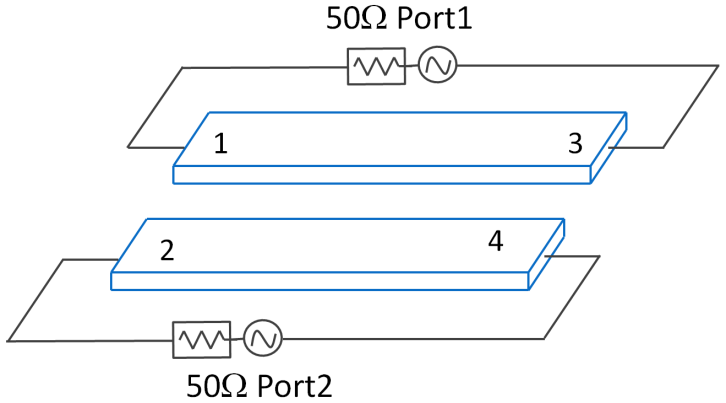
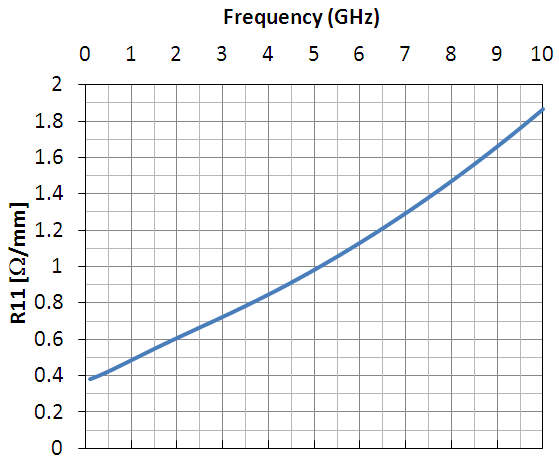
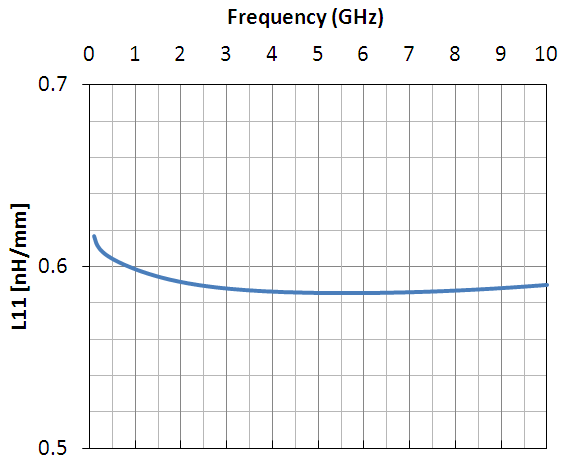


Fig. 5: Second simulated representation of the Line in Differential mode   
in order to extract the Inductive performance of the line.



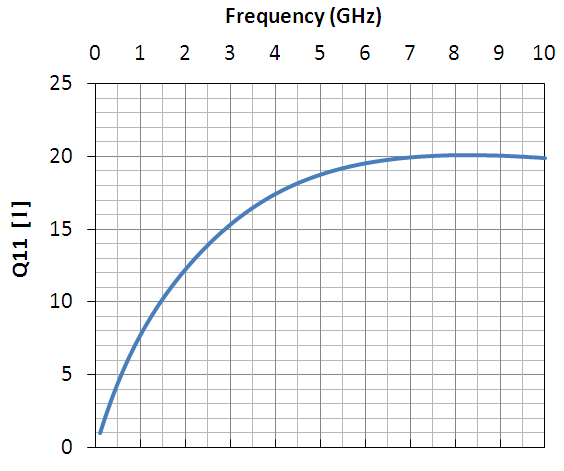
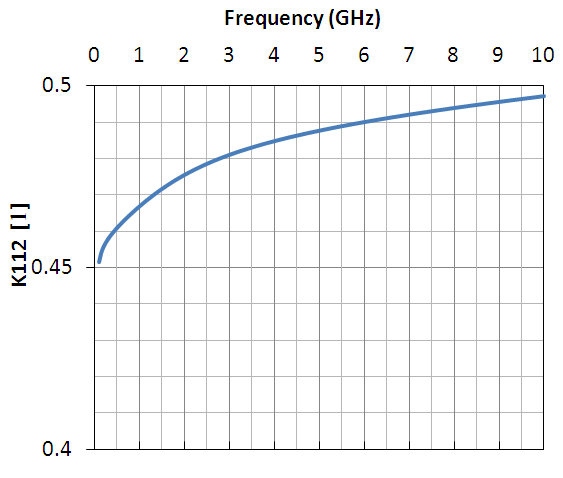


Fig. 6: Inductive Performances of the Line versus Frequency (GHz).

The Metal Line features an inductive value of 0.59nH/mm@2.45GHz, a DC resistance of 0.38/mm, a coupling factor of 0.48@2.45GHz and Q-factor of 13.8@2.45GHz. It is interesting to observe that the resistance increases versus frequency that could suggest that skin effects occur in the Line.

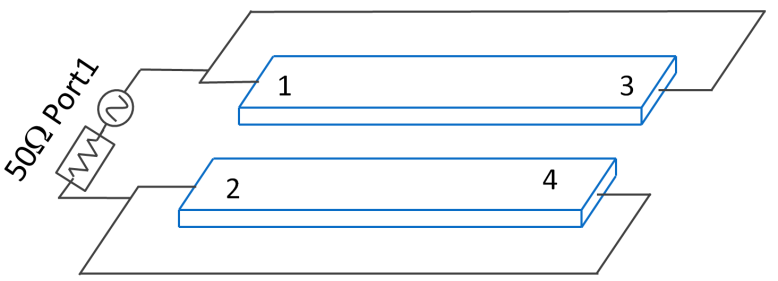


Fig. 7: Third simulated representation of the Line in Differential mode  
in order to extract the Capacitive performance of the line.

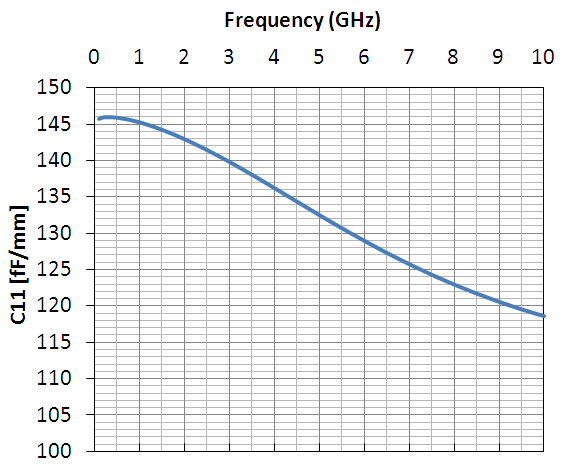
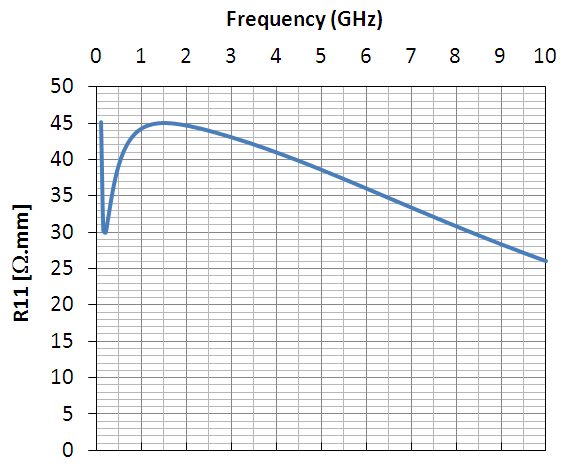
 

Fig. 8: Capacitive and Resistive Performance of the Line versus Frequency (GHz).

From Fig. 8, it is interesting to observe that there is a resistive path between the two lines and the value is quite far away from the null value. This real resistive path can be explained due to the fact that the electric field enters to the silicon. This real resistive path creates extra power losses. A good point of view could consider different conductivity of the Lossy Silicon to evaluate its influence on the losses.

1. **Conventional Differential Lines with different silicon conductivity**

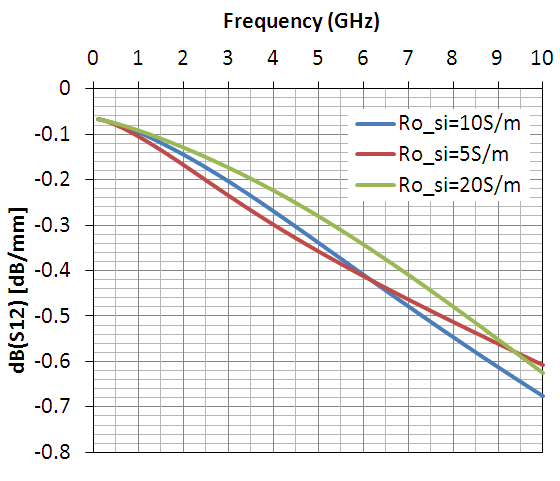
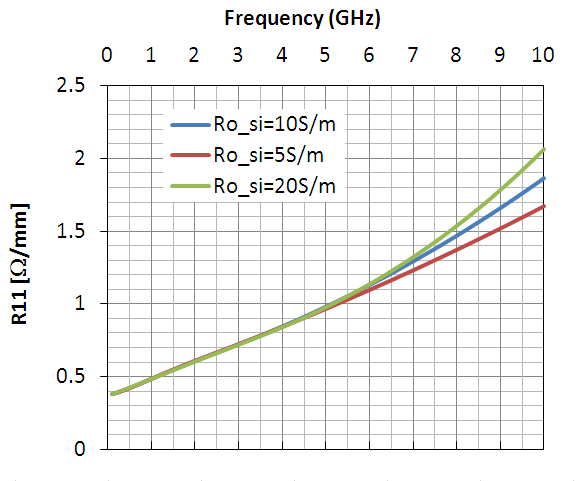
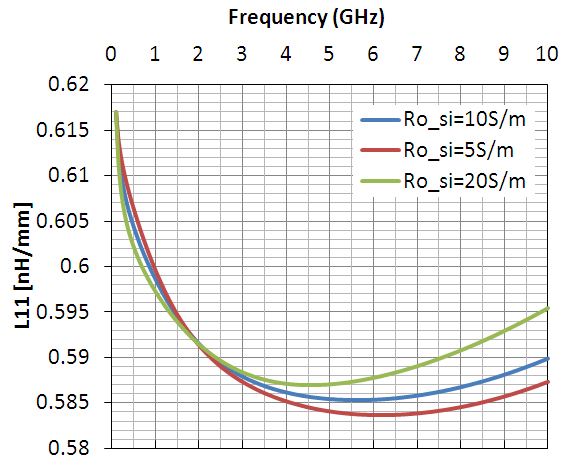


Fig. 9: Losses dB(S12) (dB/mm) versus Frequency (GHz) for different silicon conductivity.

From Fig. 9, it is interesting to observe that the losses at 2.45GHz decrease when the silicon conductivity increases (in this range of silicon conductivity). The losses are extracted to 0.197 and 0.148dB/mm for the silicon conductivity varies from 5S/m to 20S/m.



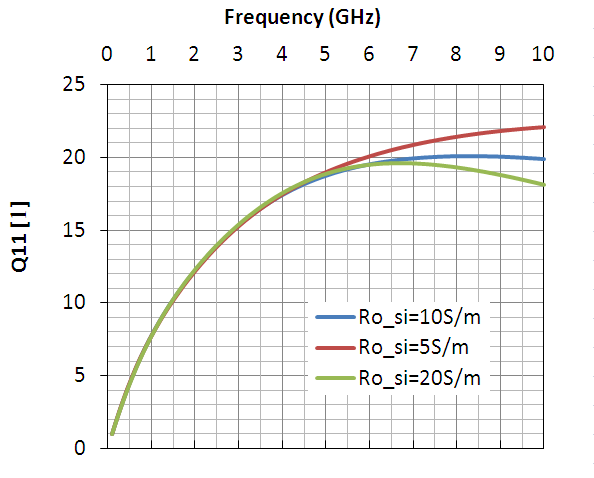
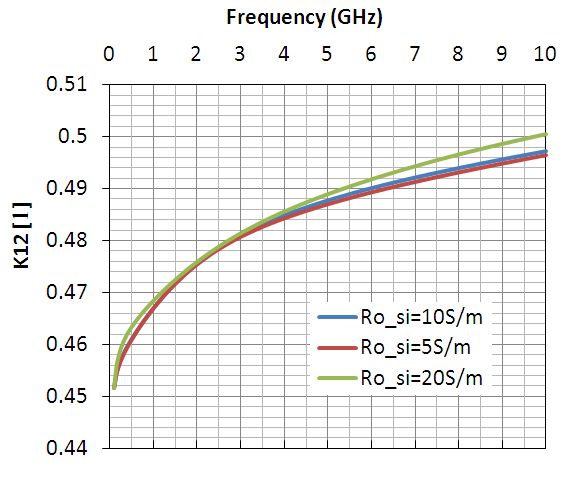


Fig. 10: Inductive Performances of the Line versus Frequency (GHz).

The silicon conductivity does not change the inductive behavior of the line. However, we can denote that the frequency at Qpeak shift decrease when the silicon conductivity increases. That may suggest that the capacitance between the two lines is higher when the silicon conductivity increases.

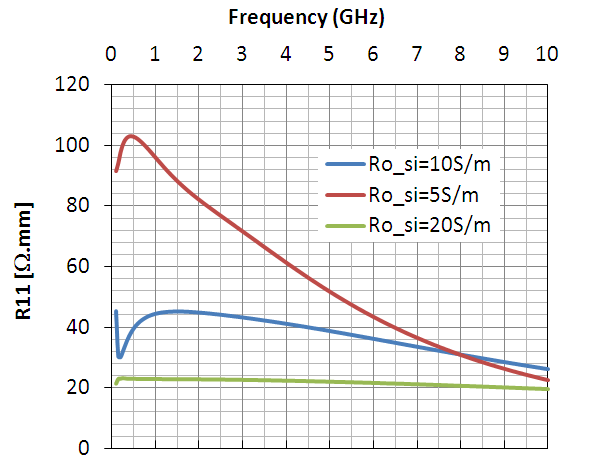
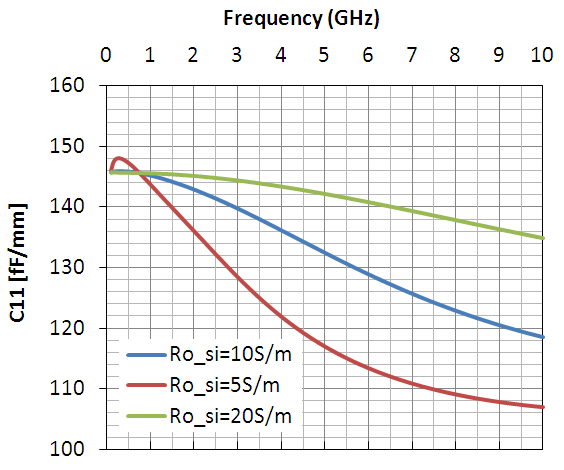


Fig. 11: Capacitive and Resistive Performances of the Line versus Frequency (GHz).

We observe that the DC capacitance is invariant. Nevertheless, in high frequency, the capacitance varies sensibly with the silicon conductivity in this range of frequency. It is confirmed that the capacitance between the two lines is higher when the silicon conductivity increases but only at high frequency. Also, the resistive path value between the two lines varies sensibly when the silicon conductivity varies. As expected, at low frequency, the resistance path value is higher when the silicon conductivity is lower, because this one is not short-cut by the silicon capacitance Csi.

Note that the variation versus frequency of the capacitance and the resistance induces that the electromagnetic power coming from the TM2 line will be distributed to different modes (i.e., other than the TEM mode).

This part may suggest that it could be interesting to increase the effective conductive path in order to decrease the line losses. A good idea could be to introduce an electric path via a metal line, enough conductive, between the TM2 lines and the silicon in order to decrease artificially the resistive path.

1. **Differential Lines with Floating Patterned Shield**

In this item, we will show the performance of the Line when a floating patterned shield is set underneath the TM2 metal lines.

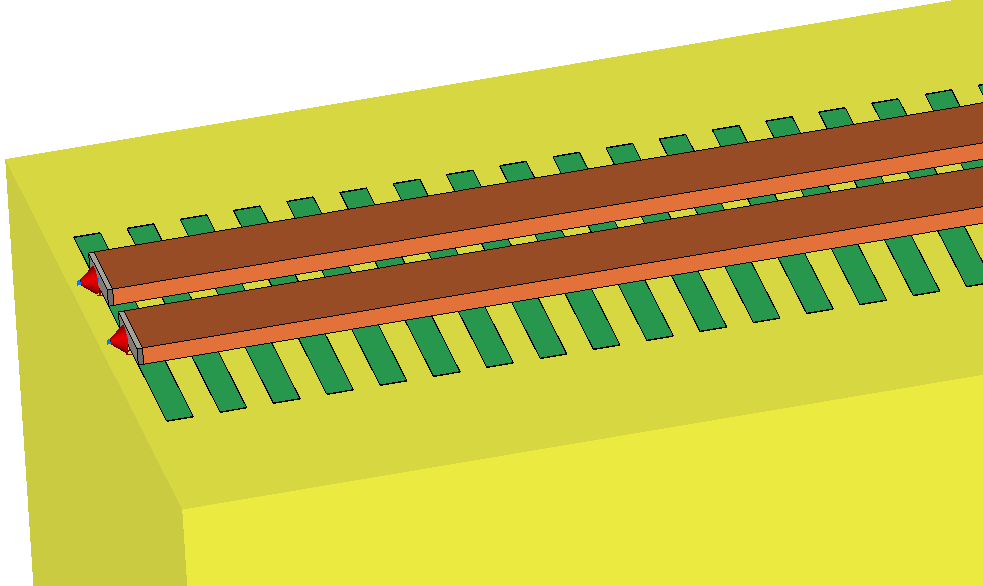


Fig. 22: 3-D Representation of the Differential Lines with Floating Patterned shield

The width of the poly line and the spacing between poly line are arbitrary chosen to 5 and 5um, respectively.

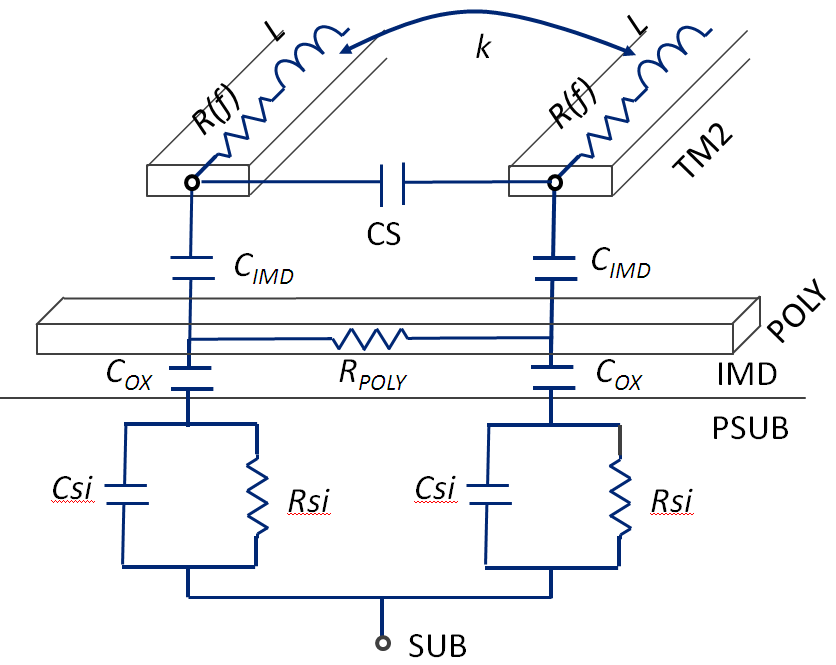


Fig. 23: Electrical Representation of the Conventional Differential Line with Pattern Layer

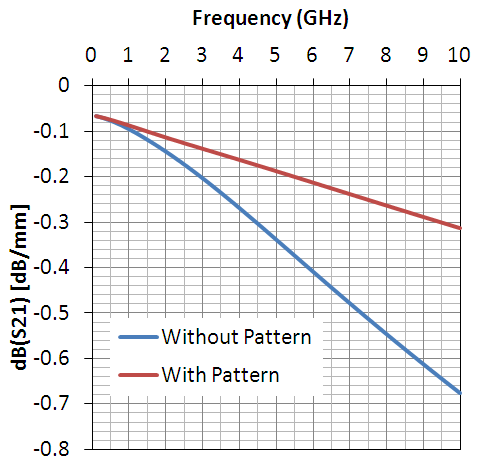
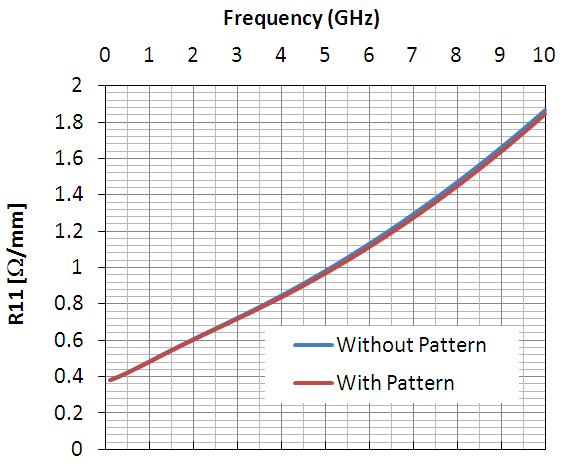
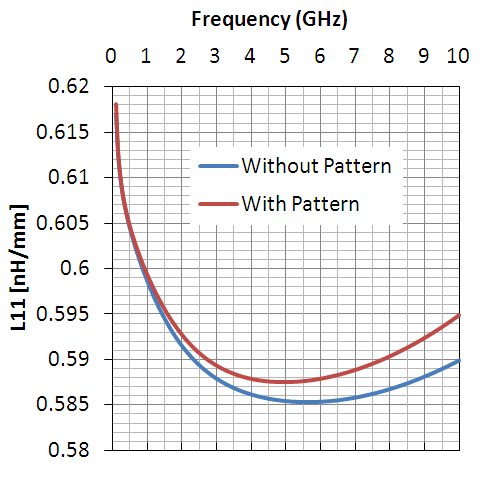


Fig. 24: Losses dB(S12) (dB/mm) versus Frequency (GHz) for the topologies   
with and without Patterned layer.

Fig. 24 shows without doubt that decreasing artificially the resistive path lead to better performance of the line. The losses with a floating patterned shield are evaluated to 0.125 and 0.185dB/mm at 2.45 and 4.9GHz, respectively whereas without the floating patterned shield, the losses are evaluated to 0.17 and 0.33dB/mm.



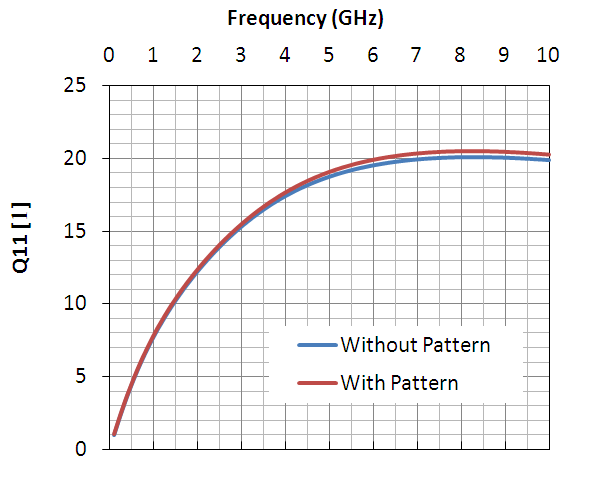
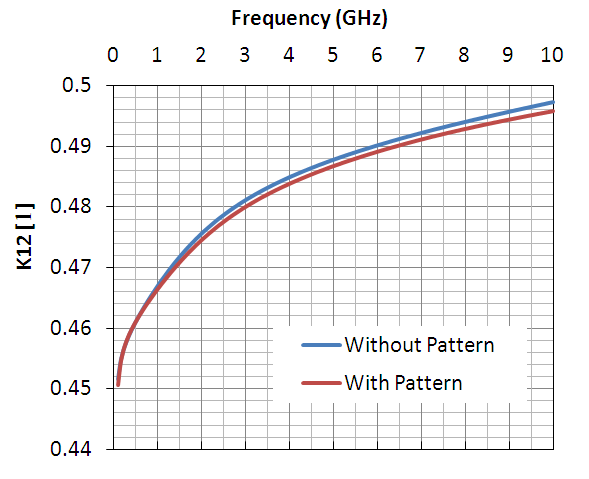


Fig. 25: Inductive Performances of the Line versus Frequency (GHz).

We can observe that the floating patterned layer does not introduce any variation on the inductive quality of the Line.

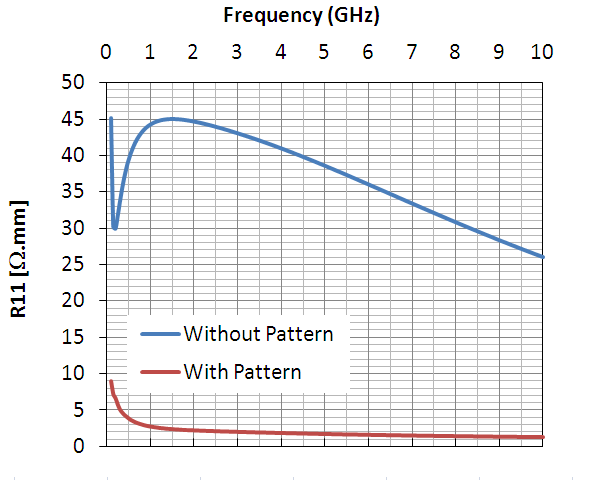
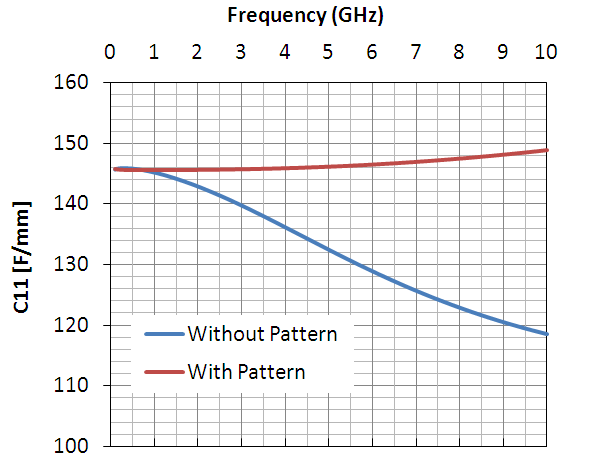


Fig. 26: Capacitive and Resistive Performances of the Line versus Frequency (GHz).

As expected, the resistive path has been decreased sensibly. In this way, the electromagnetic power dissipated out of the TM2 line is lowered and the losses of the line decrease. Moreover, the DC capacitance does not change. Nevertheless, the capacitance with a patterned shield remains almost constant versus frequency.

We can conclude that adding a floating patterned shield underneath the TM2 lines does not induce any large changes in the layout of the differential lines, but improve sensibly its performances.

Note that since most of the power go across the poly line and does not penetrate the silicon, it is expected that the high frequency noise as well as the electric and magnetic cross coupling in relation with the TM2 lines is reduced. This part requires naturally more investigations for confirmation and is out of scope of the document.

1. **Differential Lines with Floating Patterned Shield with Split Lines**

In this item, we will show the performance of the Line when a floating patterned shield is set underneath the TM2 metal lines and when the Lines are split into two Lines. This last feature is dedicated to reduce the skin effects and then reduces the linear losses of the Lines versus frequency. For more details, we would refer the reader to the last internal document about skin effects and its modeling (please feel free to ask me this document).

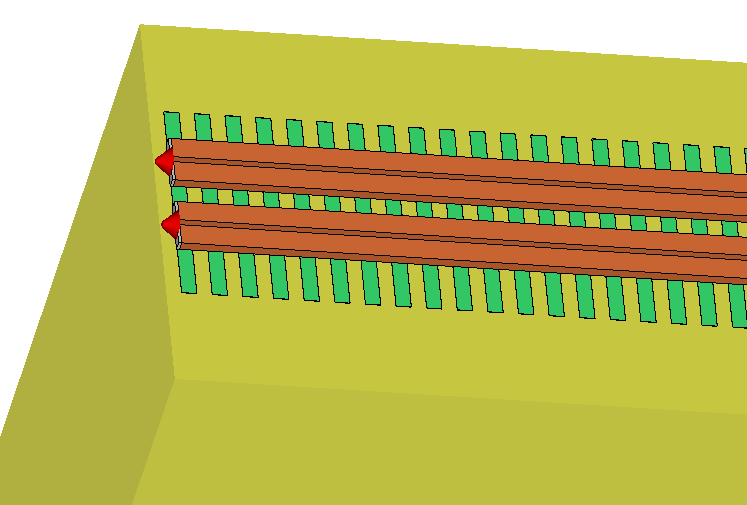
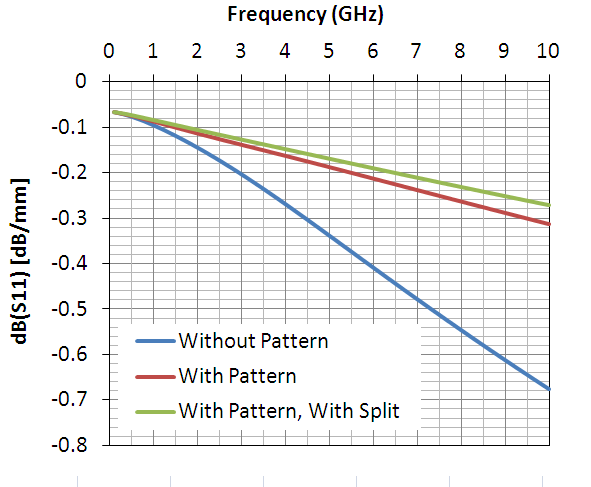


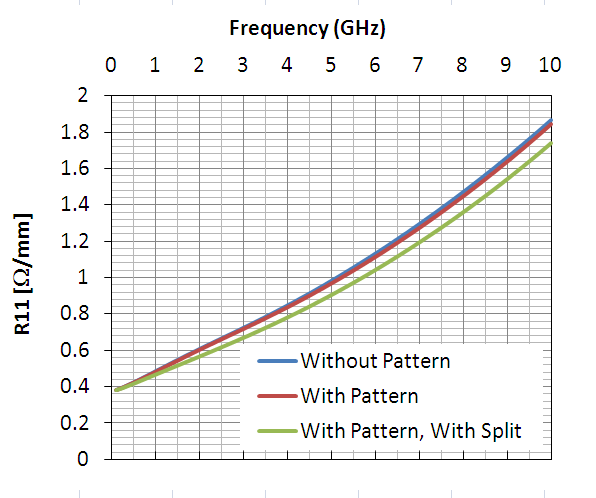
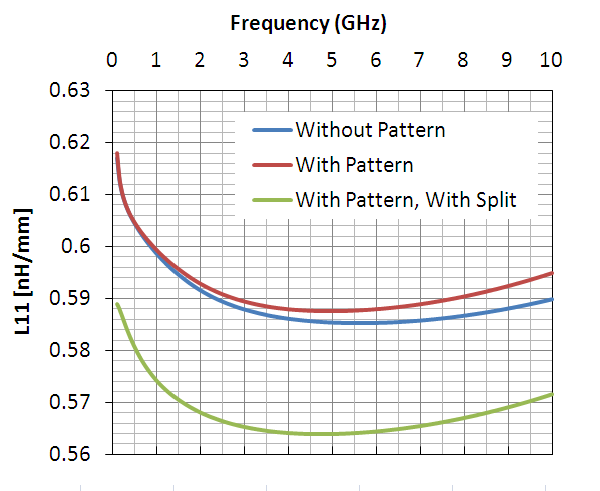
Fig. 37: 3-D Representation of the Differential Lines with Floating Patterned shield with split lines.

The split spacing between a poly line is arbitrary chosen to 3um. The total conductive width remains constant to 14.54um. In this way, the DC resistance of the Line remains constant.



**Fig. 28:** Losses dB(S12) (dB/mm) versus Frequency (GHz) for the topologies   
with and without Patterned layer.

A slight improvement on the linear losses is observed when the two TM2 lines are split into four lines. The losses with a floating patterned shield and split lines are evaluated to 0.115 and 0.167dB/mm at 2.45 and 4.9GHz, respectively whereas with the floating patterned shield but no split line, the losses are evaluated to 0.125 and 0.185dB/mm.



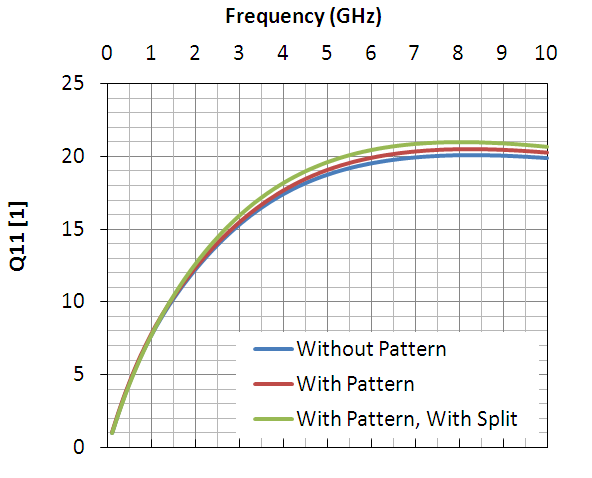
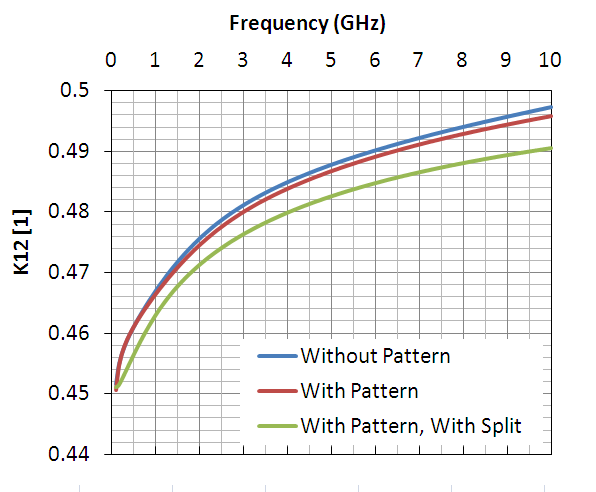


Fig. 29: Inductive Performances of the Line versus Frequency (GHz).

We can observe that the inductive behavior of the split line is a slightly different than with no split line. The inductance value and the coupling factor are slightly smaller. The resistances show a slight decrement showing that the skin effects occur less when the lines are split.

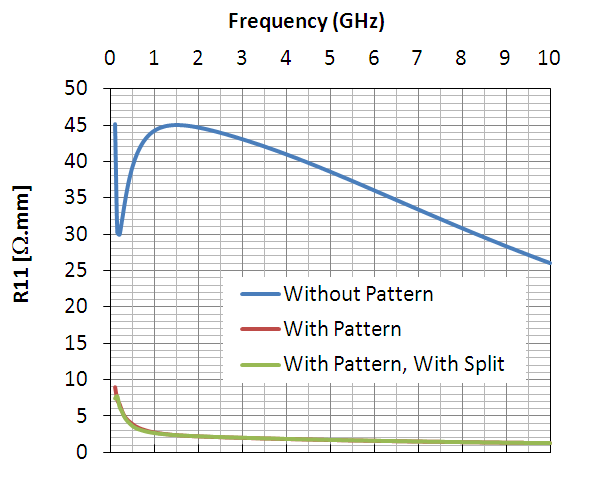
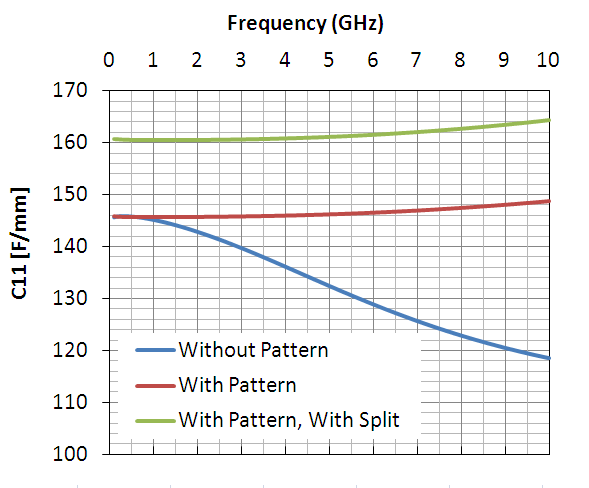


Fig. 30: Capacitive and Resistive Performances of the Line versus Frequency (GHz).

We can observe that the resistive path does not change. Also, we note that the capacitance C11 increases when the TM2 lines has been split. This could be explained by an increment of the parallel capacitance CIMD due to higher fringing field. To confirm this point, we simulate the line following the circuit configuration shown in Fig. 31 in order to extract the different components of capacitance (*i.e.*, CS and CIMD).

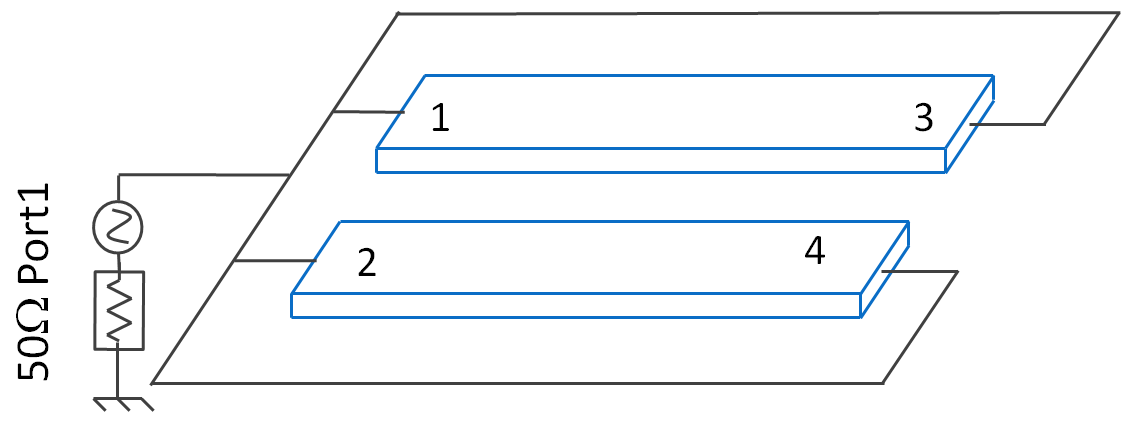
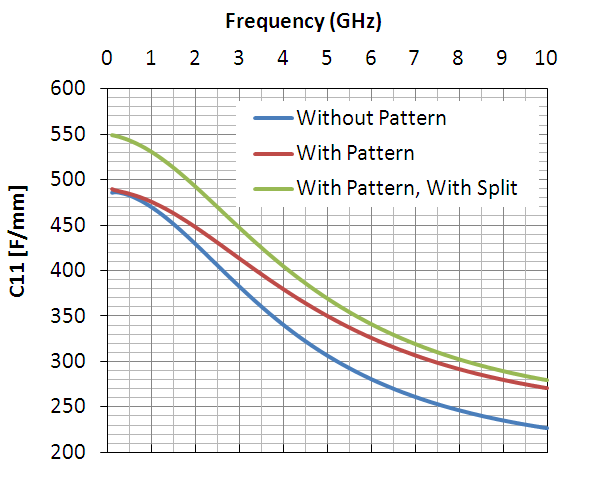


Fig. 31: Fourth simulated representation of the Line in order to extract the parallel capacitance to ground.



**Fig. 32:** Extracted Capacitance following the schematic show in Fig. 31

Considering the TM2 lines with no split, the parallel capacitance CIMD has been extracted to 243fF and coupling capacitance CS to 23.5fF. Considering the TM2 lines with split, CIMD has been extracted to 274fF and CS to 23fF. We confirm that the coupling capacitance does not change. CIMD increases due to an increment of fringing capacitances.

Note that all these results concern only differential signals. In case of single-end signal, the role played by the floating patterned layer induces different performances and it would be preferable to set a ground connection to the patterned layer.

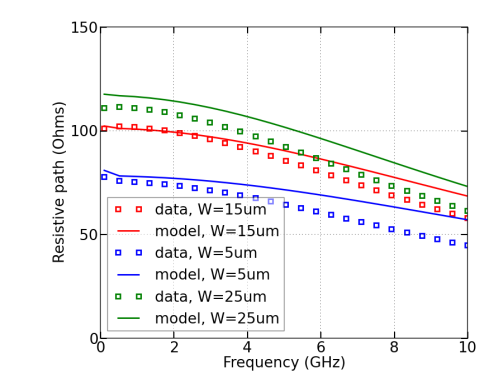
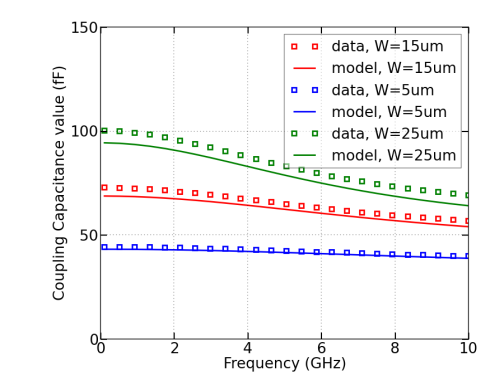
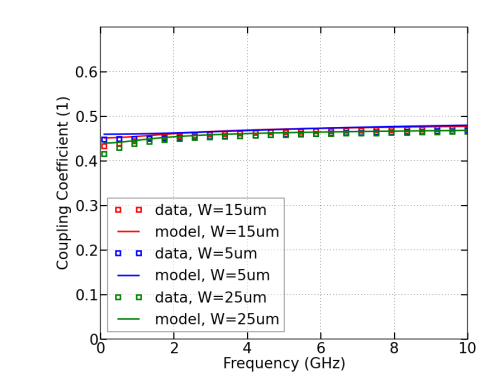
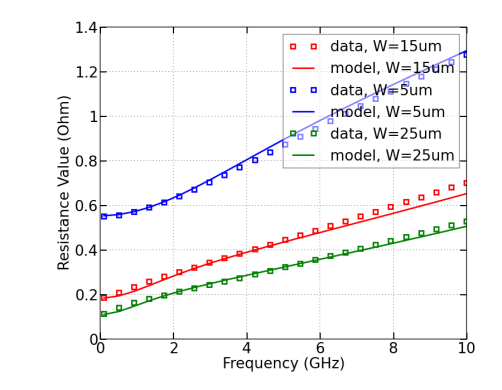
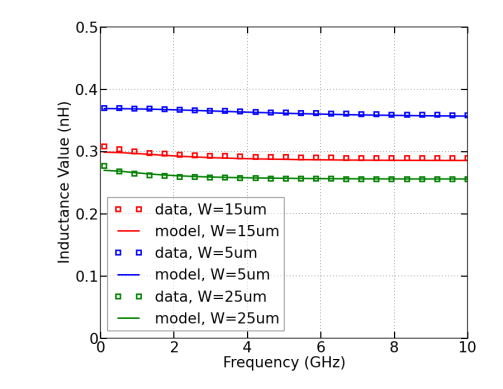
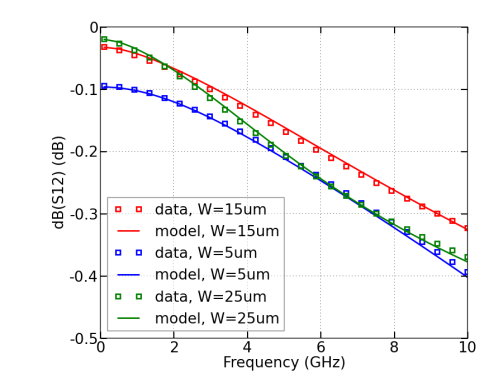
1. **Modeling**

For design purpose, we have developed full scalable (length, width, spacing) spice models based on discrete elements for the conventional Differential Lines on 10S/m silicon conductivity and for the Differential Lines with Floating Patterned Shield. It allows designers to use it in order to optimize the dimension of the Lines.

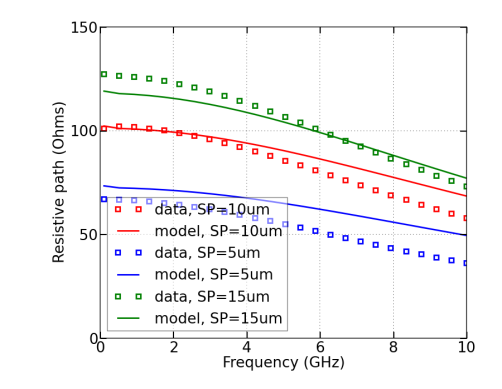
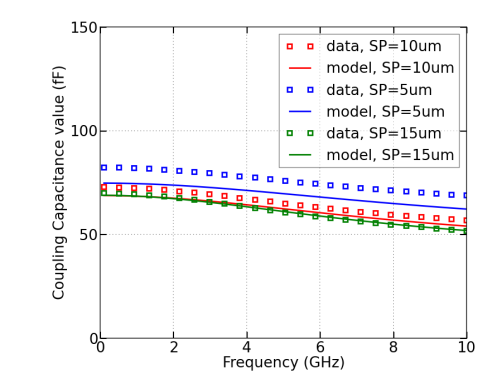
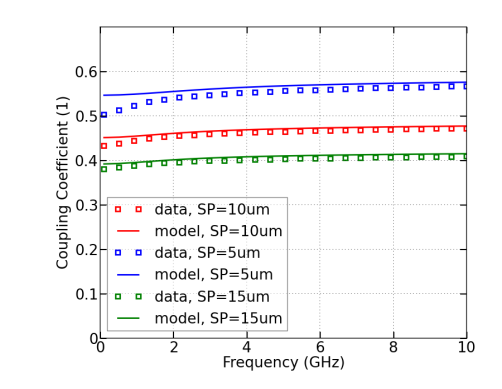
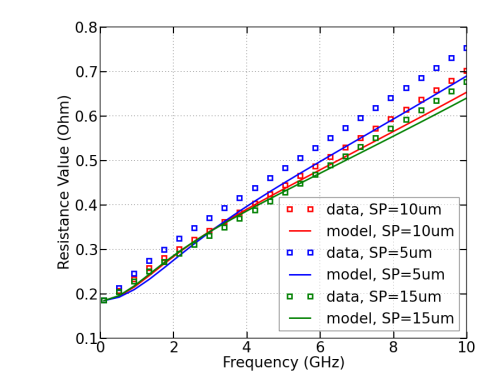
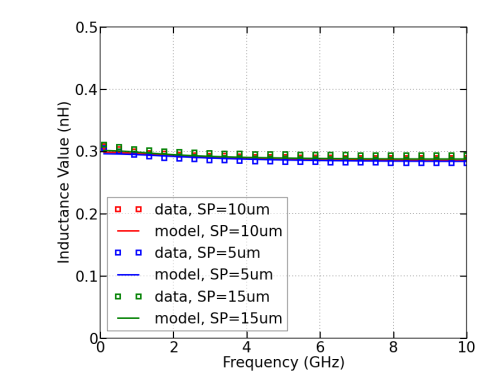
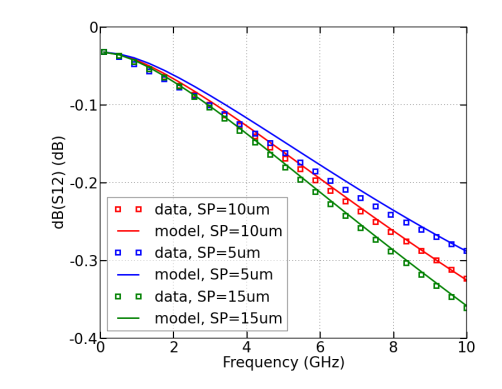
The symbols associated the model files have been created and can be inserted into the SMIC55LL PDK.

The results of the modeling are presented below:

* 1. **Conventional Differential Lines on 10S/m silicon conductivity**

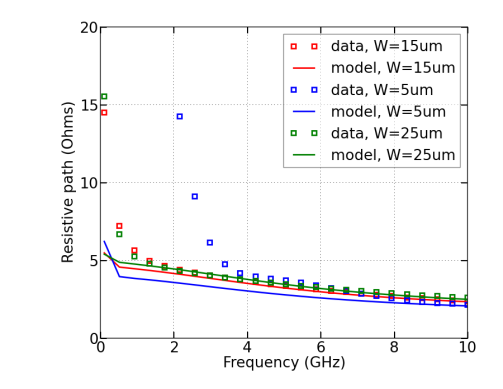
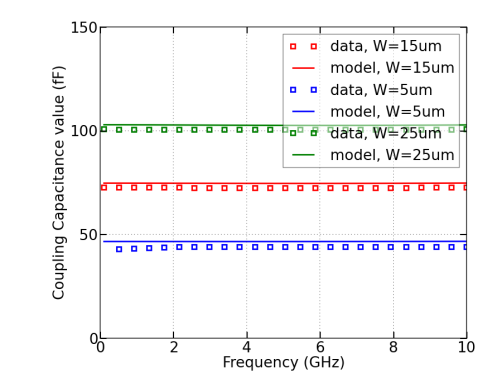
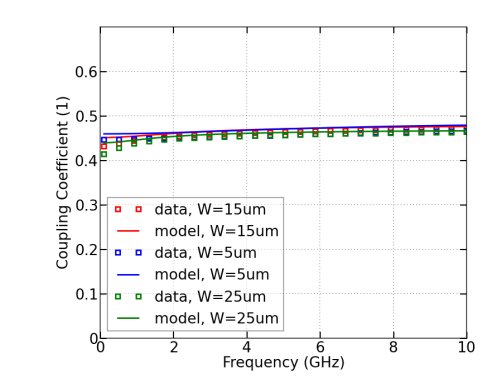
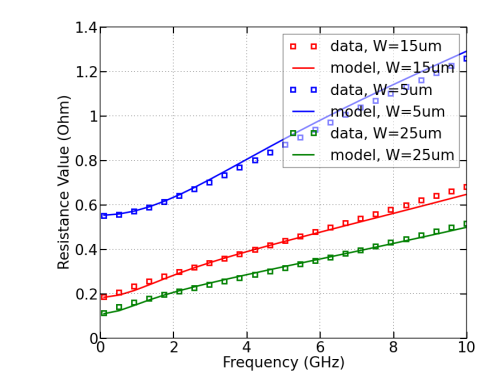
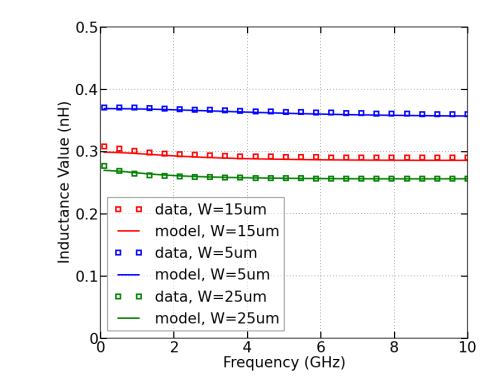
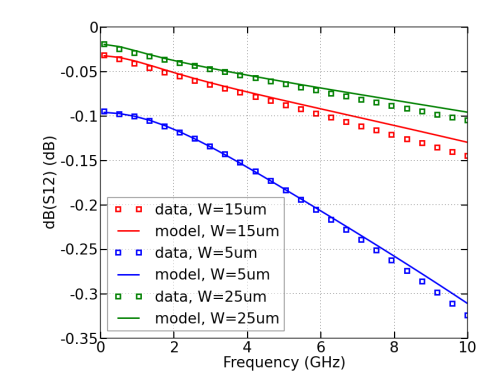


**Fig. 33:** Extracted Parameters for the Model and the Data when Spacing=10um.

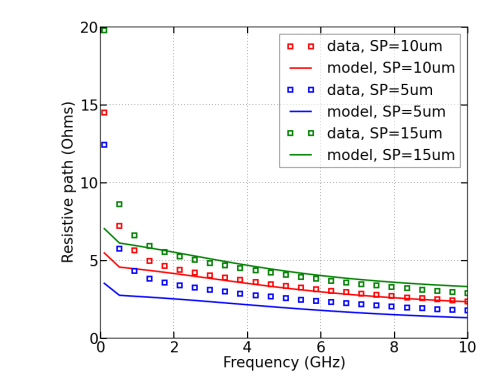
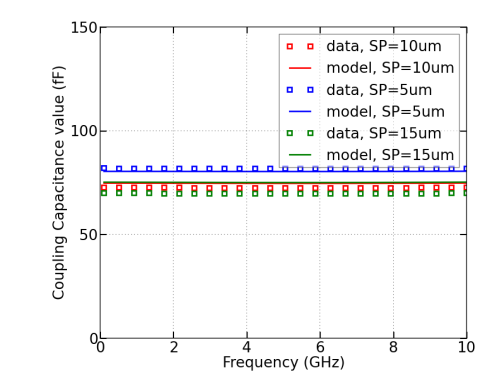
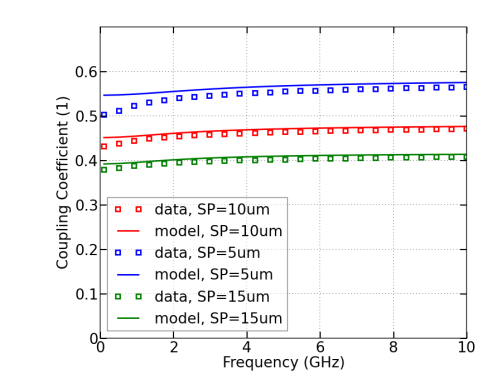
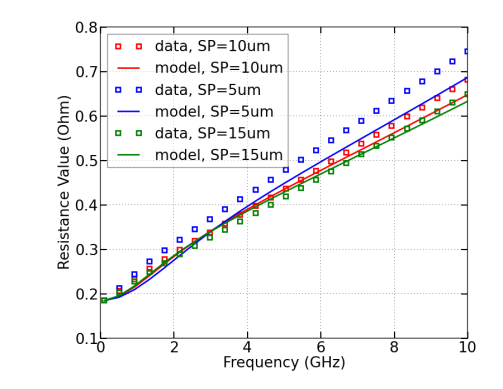
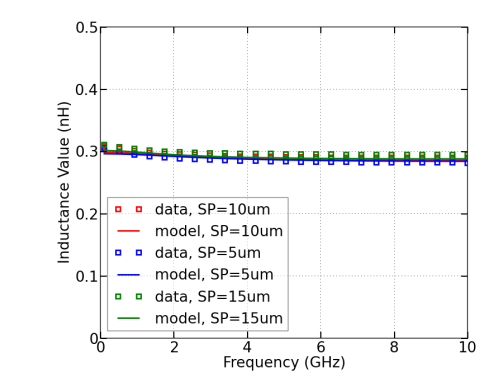
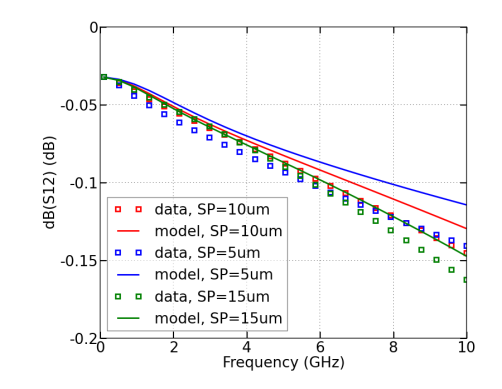


**Fig. 34:** Extracted Parameters for the Model and the Data when Width=15um.

* 1. **Differential Lines with Floating Patterned Shield**



**Fig. 35:** Extracted Parameters for the Model and the Data when Spacing=10um.



**Fig. 36:** Extracted Parameters for the Model and the Data when Width=15um.

As we can see, the extracted models compared to the data are accurate. By the way, we can observe the requirement to optimize the width and the spacing of the line to reach better performances.